Application Notes
Power Management
with OMAP EVM35xx Platform running Windows CE 6

Document purpose:

This Bsquare external document is intended to provide an overview of power management capabilities on an OMAP EVM35xx Platform running Windows CE 6.

TABLE 1. REVISION HISTORY

Revision	Date	By	Purpose
1.0	Jan 05th 2010	Joseph Lee	
1.1	Jan 10th 2010	R. Leeson	
1.2	Jan 20th 2010	R. Leeson	
1.3	Apr 12th 2010	R. Leeson	6.14.00 release
1.4	May 28th 2010	R. Leeson	6.14.01 release

I. Overview

Modern mobile computing devices use hardware and software power management techniques to control power consumption and thereby extend battery life.

This document provides a high level overview of Power Management capabilities of Windows CE6, the OMAP35xx processor family, and the OMAP EVM35xx Processor Family BSP (TI_EMV_3530 BSP).

A detailed discussion of power management is beyond the scope of this document and the reader is encouraged to consult the Windows CE6 documentation and the OMAP35xx processor family documentation for more information.

II. Windows CE Power Management Software

This section discusses, in generic terms, the power management capabilities of Windows CE6. See the Windows CE6 documentation for more information.

CPU Idle State: When the kernel scheduler is idle (no threads are ready to run) the kernel will activate BSP code that places the CPU into a reduced power state until an interrupt occurs. This may happen many times in any given second and is transparent to application and driver behavior.

Power Manager Model: The OMAP 35xx CE6 BSP uses the Power Manager model for power management rather than the add-hock methods (GWES timers, backlight timers, etc.) supported in earlier versions of Windows CE. Note that because Windows CE6 still includes vestiges of these add-hock methods, some of the documentation, control panel applications and registry entries are irrelevant or incorrect.

D States (Power States): Windows CE includes a power management subsystem that (by default) supports 5 power states from D0 (full on) to D4 (full off). Device drivers can register to receive notifications of changes to the system power state. Device drivers also have individual power states and can interact with each other to manage power state relationships.

Suspend/Resume: The Windows CE power management subsystem supports suspending the system by placing the GWES, the device drivers, and the file system manager into the D4 state. The OAL will then continue the suspend process by saving critical OMAP35xx registers, placing the CPU into a low power state to await a wake up event. After a wake up event, the process will be reversed by the resume sequence. Note that the actual suspend power state of each of the device drivers is determined by the device driver design, most will use D4 but devices that can wake the system from suspend may use D3. The Ethernet driver is an example of a driver that uses D3 for suspend.

Idle Timers: The Graphical Windowing Event Systems (GWES) works with the Power Manager (PM) to control idle timers based on user and system activity detection that can be configured to change the system wide power state. These timers are configured using registry entries.

User Idle Timer: When the user interface is idle for a period of time (configurable using registry entries), PM can change the system power state to D1. Device drivers that receive notification of system power state changes can then respond by going to a reduced power state as applicable. An example of a device driver that can be configured to respond to the D1 system power state is the backlight driver.

System Idle Timer: When the system appears to be idle for a period of time (configurable using registry entries), PM can change the system power state to D2. Device drivers that receive notification of system power state changes can then respond by going to a reduced power state as applicable. An example of a device driver that can be configured to respond to the D2 system power state is the backlight driver.

System Suspend Timer: When the system appears to be idle for an extended period of time (configurable using registry entries), PM can change the system power state to D4 causing the system to suspend.

The default association of power states to system states:

D0 Full On
D1 User Idle
D2 System Idle
D3 Off/Suspend with wake capability
D4 Off/Suspend

III. OMAP35xx Power Management Hardware

This section discusses, in generic terms, the power management capabilities the OMAP35xx processor family. See the OMAP35xx documentation for more information.

Controller Interface Clock Management: The interface clocks are used to access the registers in on-chip subsystems. To save power, interface clocks can be disabled when the registers in a subsystem are not being accessed.

Controller Functional Clock Management: The functional clocks are used to run the logic in on-chip subsystems. To save power, functional clocks can be disabled for subsystems that are not being used.

Shared Clock Management: The clock sources that are shared between several subsystems can be disabled when none of the subsystems that use the clock are being used.

Power Domain Management: There are several power domains inside the OMAP35xx CPU family. The power supplies to these domains can are switched on/off according to the PRCM subsystem register configuration and rules built into the OMAP35xx logic design. This allows the power supply to sections of the OMAP35xx chip to be shut off when not in use or when the system enters a low power state (such as during suspend).

Programmable Clock Speeds: Clocks for many on-chip subsystems can be programmed to run at different frequencies. The MPU (CPU), IVA (DSP) and core functional clocks are the most important variable speed clocks for power management. The maximum clock frequency that can be used for these blocks depend on the chip manufacturing test results (speed grade) and on the voltage being supplied to the domain that the subsystem is part of.

Programmable Domain Voltages: The OMAP35xx voltage processor can communicate with an external PMIC (Power Management Integrated Circuit) to control the voltage supplied to the OMAP35xx domains. For some domains, the domain voltage can be reduced if the functional clocks to subsystems within that domain are running at a reduced frequency. Voltage changes are important because the power consumption used by logic circuits is roughly proportional to the square of the voltage used to power the logic times the clock rate ($Power = Voltage^2 * Frequency$). Valid voltage and frequency pairs are called operating points (OPP).

Smart Reflex Data: During factory OMAP35xx chip testing, information about the clock and voltage requirements for some subsystems is collected and written to write once memory on the chip. This information can be used to fine tune the operating points for the MPU/IVA and CORE domains.

IV. BSP Power Management Software

This section discusses the power management capabilities the Windows CE6 BSP (Board Support Package) for the OMAP EVM35xx platform.

Note that some of the power management features may not be enabled in the by default, see the ti_evm_3530.bat file, Power Management Subsystem Settings, to understand and control which PM components are enabled.

Controller Interface Clock Management: Many devices drivers that are associated with a controller inside the OMAP3 CPU disable interface clocks for the controller when not accessing the registers.

Controller Functional Clock Management: Many devices drivers that are associated with a controller inside the OMAP3 CPU disable functional clocks for the controller when the controller is not being used.

PRCM Clock Management: The PRCM manager understands the relationships between clocks and maintains a reference count for each clock resource (interface clocks, functional clocks, shared clocks) to allow a shared clock to be shut off when all of the controllers that use the clock are shut down.

PRCM DPLL Management: The PRCM manager allows the frequency of some of the DPLL (Digital Phase Locked Loop) clock generators to be adjusted.

PRCM Domain Management: The PRCM manager understands the relationships between voltage domains and clock domains and tracks reference counts for domains to allow unused domains to be powered off.

Operating Point (OPP) Description: Note that the MPU and IVA (CPU and DSP) domains share the same power supply (VDD1) and are managed together. Example operating points (OPPn) are shown below. *See the BSP inc\bsp_opp_map.h file for details about the currently supported OPPs.* The maximum OPP that the OMAP35xx can support depends on the chip version and grade. Note that if the Smart Reflex management is active, the actual voltages used may be altered according to the SmartReflex data provided by the OMAP35xx chip.

MPU/IVA OPPs:
OPP1: VDD1 = 0.975 V, MPU = 125 MHz, IVA = 90 MHz
OPP2: VDD1 = 1.000 V, MPU = 250 MHz, IVA = 180 MHz
OPP3: VDD1 = 1.200 V, MPU = 500 MHz, IVA = 360 MHz
OPP4: VDD1 = 1.275 V, MPU = 550 MHz, IVA = 400 MHz
OPP5: VDD1 = 1.350 V, MPU = 600 MHz, IVA = 430 MHz
OPP6: VDD1 = 1.350 V, MPU = 720 MHz, IVA = 520 MHz

CORE OPPs:
OPP1: VDD2 = 1.050 V, CORE = 166 MHz
OPP1: VDD2 = 1.150 V, CORE = 332 MHz

Operating Mode Description: The operating points of the MPU/IVA and CORE are managed together as the OPM (Operating Mode) of the chip. Example operating points (OPMn) are shown below.

OPM0: MPU/IVA OPP1, CORE OPP1
OPM1: MPU/IVA OPP1, CORE OPP2
OPM2: MPU/IVA OPP2, CORE OPP2
OPM3: MPU/IVA OPP3, CORE OPP2

OPM4: MPU/IVA OPP4, CORE OPP2
OPM5: MPU/IVA OPP5, CORE OPP2 (default)
OPM6: MPU/IVA OPP6, CORE OPP2

Operating Mode Control: The bootloader sets a default operating mode using the BSP_OPM_SELECT variable set in the BSP configuration batch file. Note that if the power management software (below) is enabled then the initial operating mode used by the OS may be different that set by the bootloader (controlled by registry entries), and may even vary based on system activity.

Dynamic Voltage and Frequency Scaling (DVFS): Allows the operating mode (see above) to be changed while the system is operating. Domains controlled by this system are the CORE and the MPU/IVA (CPU/DSP) domains. The OMAP35xx PRCM subsystem is used to send commands to the external PMIC to control the domain voltages and the PRCM DPLL management capability is used to change the domain frequency. This driver is controlled by the ti_evm_3530.bat file BSP_NODVFS variable, check the .bat file to see if it is enabled. See platform.reg entries for [HKEY_LOCAL_MACHINE\OMAPPMX\Constraints\DVFS] for configuration options - "OpmInit" (sets starting OPM), "OpmFloor" (sets min OPM), "OpmCeiling" (set max OPM).

CPU Load Policy Management: This power policy subsystem is configurable using registry entries and uses information about the CPU load (ratio of time the CPU spends running code as opposed to being in the CPU Idle State) to select a DVFS state for the CORE and MPU/IVA domains. This driver requires the DVFS driver. See platform.reg entries for [HKEY_LOCAL_MACHINE\OMAPPMX\Policies\CPULOAD] for configuration options. This driver is enabled/disabled using the BSP_NOCPUPOLICY variable in the ti_evm_3530.bat file.

Device Monitor Policy Management (DEVMON): This power policy subsystem listens for device state changes and tries to ensure that the OPM (Operating Mode) stays high enough for the active devices to operate correctly. This driver requires the DVFS driver. Note that this driver also controls the lowest OMAP35xx state that the chip can enter during suspend. See the platform.reg entry at [HKEY_LOCAL_MACHINE\OMAPPMX\Policies\DEVMON], SuspendState. Note that the actual state entered by the CPU during suspend may be higher than the SuspendState due to hardware or software constraints. Note that if DEVMON is not enabled, then the suspend state is controlled by the initial value of the _suspendState variable in src\oal\oallib\oem_latency.c.

DEVMON uses omap35xx_tps659xx_ti_v1\omap\pm\policyadapters\devmon\devoppmap.h information to set the minimum OPM allowed when a device is active. Note that the default values in this file constrain the minimum OPM to OPM1 when any of the MCBSPn device clocks are active and to OPM2 when any of the USB device clocks are active. Note that reducing the minimum OPM values for these devices may reduce power consumption for systems that do not use or can tolerate some reduction in performance for the MCBSPn and USB devices.

Interrupt Latency Constraint Management: Places constraints on the DVFS operating mode and the state used when the CPU Idle State is entered. This system uses information about unmasked interrupts and the maximum interrupt latency that each interrupt can tolerate to prevent the CPU from being placed into a state where interrupt latency times are too high for proper operation of the device associated with the interrupt. The configuration of this feature is fixed in the OAL (no configuration options). This feature is part of DVFS.

System State Policy Manager: Provides constraints on the DVFS operating mode based on user activity (see Platform Builder help for more information by searching for “UserIdle”).

Smart Reflex Policy: This subsystem uses information written into write once memory in the OMAP35xx chip during factory testing. This information describes fine tuning that can be done to the OPPs (Operating Points). This driver requires the DVFS driver. This driver is enabled/disable by the BSP_NOSMARTREFLEXPOLICY variable in the ti_evm_3530.bat file.

V. Device Driver Specific Power Management Software

Some device drivers employ power management techniques that are not specific to either Windows CE6 or to the OMAP35xx family CPU design.

Display Driver Low Power Refresh: When driving only an LCD (Liquid Crystal Display) panel, the display driver may change the clocks used by the display controller to reduce power consumption. This may change the LCD refresh rate, but this will have no visual effect on modern active matrix LCD panels.

Device Driver Power Internal Management: Many device drivers directly manage the power consumption of resources used by the driver. This may be done independent of the system power state or the driver power state. Examples would be controlling clocks and power for the MMC/SD/SDIO socket or placing an external chip into low power mode when the driver is idle.

VI. Suspend/Resume

The EVM can be caused to suspend using:

Desktop Start button menu, "Suspend" command.
SetSystemPowerState(NULL, POWER_STATE_SUSPEND, 0) function call.
Press the OMAP_PWR button.
GWES suspend timer timeout (disabled by default, but can be enabled by registry entries).

The EVM can be caused to resume using:

RTC (Real Time Clock) Alarm (EVM2 only).
OMAP_PWR button.

Note that early versions of the TI_EVM_3530 BSP enabled resume using one or more of the 3 by 5 matrix of buttons near the display. Recent versions of the BSP disable this feature in favor of using the OMAP_RST button near a corner of the board. See the platform.reg file, [HKEY_LOCAL_MACHINE\Drivers\BuiltIn\Keypad], EnableWake registry entry to see if the version of the BSP you are using has keypad wake enabled or to change the behavior.

VII. Measuring Power Consumption

The TMDSEVM3530 and TMDXEVM3503 platforms have some provisions for measuring power consumption of individual power supplies by measuring voltages using 2 pin headers on the main board. Note that a voltmeter with a millivolt (mV) range may be needed for accurate measurements. See the main board schematics for more information about these power measurement points.

Control of the OPM: The operating mode can be controlled using the Platform Builder target control shell "opm" command. This requires an image that supports KITL and has DVFS enabled (BSP_NODVFS not set).

If CPULOAD policy is enable (BSP_NOCPUPOLICY not set) the OPM (and VDD1 and VDD2 voltages) may vary according to system activity. Use of the Target Shell OPM command with the "-f" option may help to keep the voltages at fixed levels. If that does not work, then a special build (with BSP_NOCPUPOLICY set) may be needed.

VDD1: Measure voltage between ground and a pin on J6. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J6 then dividing that voltage by 0.05 (value of the resistor in parallel with J6) to compute the current.

VDD2: Measure voltage between ground and a pin on J5. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J5 then dividing that voltage by 0.1 (value of the resistor in parallel with J5) to compute the current.

VIO: Measure voltage between ground and a pin on J9. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J9 then dividing that voltage by 0.1 (value of the resistor in parallel with J9) to compute the current.

VIO (CPU): Measure voltage between ground and a pin on J28. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J28 then dividing that voltage by 0.1 (value of the resistor in parallel with J28) to compute the current.

VPLL1: Measure voltage between ground and a pin on J20. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J20 then dividing that voltage by 0.1 (value of the resistor in parallel with J20) to compute the current.

VBAT_OSK: Measure voltage between ground and a pin on J3. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J3 then dividing that voltage by 0.02 (value of the resistor in parallel with J3) to compute the current.

USB_3V3: Measure voltage between ground and a pin on J12. Note that one pin will be a slightly higher voltage than the other, use the higher voltage. Measure the current by measuring the voltage across J12 then dividing that voltage by 0.02 (value of the resistor in parallel with J12) to compute the current.

DCIN: This power measurement cannot be performed without additional equipment to connect power to the DCIN jack of the EVM. If this is attempted, be sure that the voltage and polarity used match that of the supplied AC adapter. Use a bench power supply set to 5V to supply DCIN and measure the current supplied by bench supply.

Typical Suspend State Power Measurements:

Typical suspend power consumption measurements (below) are for the TMDSEVM3530 and the TI_EVM_3530 BSP 6.14.01 release, DVFS disabled, OPM5, no device inserted in the USB EHCI port, and nothing connected to the serial ports.

DCIN =	301 mA @ 5V	
VDD1 =	0.1 mA @ 1.35V	(J6 0.05 Ohms)
VDD2 =	0.5 mA @ 1.15V	(J5 0.1 Ohms)
VIO =	87 mA @ 1.8V	(J9 0.1 Ohms)
VIO (CPU) =	23 mA @ 1.8V	(J28 0.1 Ohms)
VPLL1 =	7.3 mA @ 1.8V	(J20 0.1 Ohms)
VBAT_OSK =	44 mA	(J3 0.02 Ohms)
USB_3V3 =	15 mA @ 3.3V	(J12 0.02 Ohms)

VIII. Known Power Management Issues

TMDSEVM3530 and TMDXEVM3503 Design: Some elements of the hardware designs limit the ability of the power management system to control power consumption, particularly in suspend. Examples include the Ethernet chip (no suspend mode), the video capture chip (power down pin not controlled), serial port level shifters (always on), power supplies/LEDs that are always on, and use of an EHCI USB port transceiver chip that has incompatibilities with the EHCI ULPI interface that prevent the USB bus from being placed into suspend mode . See the TMDSEVM3530 and TMDXEVM3503 schematics for more information.

Interrupt Latency: When the CPU enters the wait for interrupt state during idle periods (OEMIdle), the amount of time required for the CPU to return to normal operation and service an interrupt will depend on the configuration of the Interrupt Latency Constraint Management subsystem. If the interrupt latency times are longer than required, the configuration will have to be modified.

OPM6 Support: The BSP is configured for a maximum OPM of OPM5. Changes to the registry will be needed to enable full support for OPM6. Note that it is not known if the SmartReflex system will operate correctly with OPM6.

DSP Subsystem: The DSP subsystem does not interact with the power management subsystem running on the MPU. If the MPU is load is light, the OPM may be lowered even when the DSP load is high. This may be an issue because the MPU and DSP subsystems are controlled together when the OPM changes.

See the BSP readme.txt for other known issues.

IX. More Information

For more details regarding Windows CE and OMAP35xx Power Management refer to the sources in the reference list (below) and to the release notes that accompany the BSP.

X. References

1. CE Power Management
2. Power States
3. System Power States
4. System Power State Transitions
5. Suspend State

6. Suspend Timeout Support
7. Suspend and Resume Power Callbacks
8. Power Manager Suspend Timeouts
9. Device Driver Interface
10. Windows Mobile Power Management Explained
11. Windows CE Power Manager
12. OMAP35x Family of Products TRM (Technical Reference Manual)
13. OMAP35x Power, Reset and Clock Management TRM
14. EVM 3530 BSP User Guide
15. For more information, go to http://wiki.omap.com/index.php?title=WinCE#Information_Links
16. For help and support, go to http://www.bsquare.com/omap3

XI. Appendix – Power Consumptions with Typical Use Cases

The following table contains the power consumptions measured with the EVM2 platform using CE6 BSP 6.14.00 Release in a test laboratory setup environment.

User Scenario	DVFS	Smart Reflex	Power (mW)
Audio Playback Playing an MP3 file from SD card using Windows Media Player to the loudspeaker	off	off	198.6594
	on	off	135.2286
	on	on	117.1614
Audio/Video Playback (H.264, AAC) Playing a video files from SD card using Windows Media Player. Display goes to LCD screen, audio to the loudspeaker	off	off	595.9082
	on	off	457.3895
	on	on	401.1491
Audio/Video Playback (MPEG4, AAC) Playing a video files from SD card using Windows Media Player. Display goes to LCD screen, audio to the loudspeaker	off	off	539.9437
	on	off	426.5061
	on	on	365.0063
System Suspend Remove attached peripherals, press the button and place the system in Suspend mode	off	off	76.8416
	on	off	33.35677
	on	on	33.1372